AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning on page 11, line 22 with the following amended paragraph:

On the upstream packet path, the AFE PAD includes a first-in-first-out (FIFO) buffer 400 where upstream packets from the AFEs are stored and a cyclic prefix remover 404. After removal of the cyclic prefix each packet is then passed to the DFT mapper 424. The DFT mapper is coupled to the input memory portion of the FTE via a multiplexer 420. The mapper handles writing of each sample set from a packet into the input memory in the appropriate order. The mapper may also handle such additional functions as time domain equalization (TEQ) filtering which is a digital process designed to normalize the impact of differences in channel response. The filter may be implemented as a finite impulse response (FIR) filter. The input memory comprises two portions 416 and 418. Multiplexer 420 provides access to these memories. While one sample set, e.g. time or frequency domain data, is being written from the upstream or downstream data paths into one of the memories the contents of the other of the memories are written into the row and column component 412 of the FTE 322. Once the DFT is completed by the row and column component the frequency domain coefficients generated thereby are stored in either of portions 408-410 of the output memory of the FTE. These coefficients correspond with each of the DMT subcarriers. A multiplexer 408 handles the coupling of the output memory to either the next component of the upstream path, i.e. the deframer-decoder 332 or of the downstream path. Next on the upstream path, the device packet with header and data portions and optional control portion is passed to the remaining components of the upstream path. These include the gain scalar and optional forward error correction (FEQ) ~~424~~ 426, the decoder ~~426~~ 428, the tone re-orderer ~~428~~ 430 and the deframer ~~432~~ 434.

Please replace the paragraph beginning on page 12, line 11 with the following amended paragraph:

A multiplexer ~~430~~ 432 couples the deframer input to either the tone ~~reordered 428~~ reorderer 430 or to the output memory of the FTE. Each of these components is individually configurable on a per channel basis using tables stored locally in registers within each component, or within memory 328. The access to these tables/registers is synchronized by the logic in each of the components which responds to header or control information in each upstream packet to alter tone ordering/re-ordering, gain scaling constants per-tone per-channel, and FEQ constants per-tone per-channel. The processor 334 may initialize all the registers. From the deframer packets are passed to the FIFO buffer 450 which is part of ATM PAD 340.

Please replace the paragraph beginning on page 22, line 15 with the following amended paragraph:

FIG.12B is a timing diagrams showing the timing associated with the row and column transforms of the IDFT. An input exhibiting hermetian symmetry is shown. The input array of frequency domain samples 850 is folded into a two dimensional array with 64 columns and after removing the lower conjugates 866 has 33 rows remaining. Each row, e.g. row 870 of the array is subject to a sliced radix transform which results in a solution to a slice of the inner nested summation shown in Equation 2 above. In the embodiment shown, the sliced radix is order "4". The row engines output comprises 4 sequential transforms1252, 1254, 1256 and 1258 of a slice of each of the row transforms. Although collectively these are equivalent in processing steps to a full radix solution they have the visible benefit of allowing column processing to begin at time t_1. If the radix input to the row engine fully completed all possible vectors, i.e. the set of 16 complex solutions for each of the 4 samples presented to it, then processing of the columns could not begin until t_4. As indicated in FIG. 12B the ordering of the slices is important as well. Two parallel column transforms are performed on slices 0,1 and 2,3 as shown on lines ~~1252~~ 1262 and ~~1254~~ 1264 respectively. The transformed output of time domain samples is written to memory starting with the first column 874. On

the first slice 1252 of all rows in the input sample set, ¼ of the columns in the output array 854 are generated. After 3 more passes 1254, 1256, 1258 through the input array the row and column transform is complete.

Please replace the paragraph beginning on page 23, line 1 with the following amended paragraph:

FIGS. 13AB are hardware block diagrams showing alternate embodiments of the Fourier transform processor of the current invention. In the embodiment shown in FIG. 13A a single sliced radix module is shown. That module includes parallel input radix processor 1300, complex scaler 1302, multiplier 1304 and twiddle factor generator 1306. The sliced radix module accepts order "R" parallel inputs from the input sample delivery circuit which in this case includes input memory 416/418 and more generally the entire downstream/transmit path or the upstream/receive path discussed above in connection with FIGS. 3-4. In alternate embodiments of the invention where the FTE may be implemented on one or the other of the upstream or downstream X-DSL paths. In still other embodiments of the invention the FTE may be used in fields other than communications such as medical imaging, pattern recognition, signal analysis, etc. In all cases the phrase input sample delivery circuit applies to whatever circuit, hardware or software which delivers sample sets to the FTE. The sliced radix module couples to the input of the row and column circuit. In the embodiment shown that circuit comprises the remainder of the row transform 1310, row/column memory 1326-1328 column transform 1330, and switched outputs 1382-1384. The coefficients, e.g. time or frequency domain are passed to output memories ~~408~~ 412 or 410. For a sliced radix "R=4" module at the input, four passes through the rows in the input memory are required to generate a complete row and column transform at the output. This results from the fact that as discussed above, only one set of 4 of the possible 16 complex coefficients or vectors is generated by the sliced radix module on each pass through the input array.

Please replace the paragraph beginning on page 23, line 21 with the following amended paragraph:

In the embodiment shown in FIG. 13B four RC modules ~~412~~ 414A-D are shown. Each has a sliced radix module coupled to the input sample delivery circuit on the input and to a corresponding row and column circuit on the output. The use of the 4 sliced radix modules in a number equal to an order R=4 of the sliced radix results in the requirement of only one pass through in the input array to generate the entire transformed output in memory ~~408~~ 412/410 .

Please replace the paragraph beginning on page 24, line 12 with the following amended paragraph:

The output from RC memory is passed to the first stage 1336 of two column transform stages 1336-1338. In the first stage a radix "R" 1352 and associated twiddle driver 1360 provides an output to multiplier 1354. The output is scaled by the multiplier with a twiddle factor 1362 and the resultant is passed to the input of a variable order radix 1356 with an order also variable between Rmax and Rmin. In the example shown Rmax = 16 and Rmin = 2. That variable order radix couples with the associated twiddle factor generator 1364. The transformed output of the variable order radix is passed via switch 1358 to the second stage module 1338. Within the second stage module switch 1366 couples the input to the positive input of summer 1372 together with the positive input of differencer 1376 or to complex conjugator 1370. The output of the conjugator is stored in a delay buffer 1370. The output of the delay buffer provides the other inputs to the summer and differencer. The timing of the switch 1366 during processing of the column portion of the two dimensional DFT has been discussed above in connection with FIG. 12A. The output of the differencer is scaled using a input from twiddle generator 1378. The scaled output provides one of the inputs to summer 1380. The other input to that summer is the output of the first stage summer 1372. The output of the second stage summer is coupled via switch 1384 to either of output memories ~~408~~412-410 (See FIG. 4). A second input to output memory is provided by complex

conjugator which is also coupled to the output of the second stage summer. This injects hermetian symmetry into the frequency domain coefficients of the output sample set stored in output memory.

Please replace the paragraph beginning on page 25, line 10 with the following amended paragraph:

The output from RC memory is passed to the first stage 1336 of the column transform as discussed above in connection with the DMT . The output from the RC memory is also provided via switch 1332 to a second first stage module 1334 which performs similarly to the first albeit with different slices to compute (See FIG. 12B). The outputs of the first stage and the second first stage are supplied to output memory via switches 1382-1384 respectively. This real valued time domain coefficients are stored in either of output memories ~~408~~ 412/410.